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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,320	12/31/2003	Edward A. Burton	884.C02US1	4675
21186	7590	06/14/2005	EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402-0938			TRA, ANH QUAN	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/750,320

Applicant(s)

BURTON ET AL.

Examiner

Quan Tra

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 December 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 21-25 is/are allowed.
- 6) ☒ Claim(s) 1-20 and 26-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1- are rejected under 35 U.S.C. 102(b) as being anticipated by Mizuno et al. (USP 6166577).

As to claim 1, Mizuno et al. discloses in figure 12 an apparatus comprising: a substrate (inherent); a target timing circuit (OSC10) formed on the substrate, the target timing circuit having a frequency related to a target frequency; a leakage timing circuit (OSC20) formed on the substrate, the leakage timing circuit having a frequency related to a leakage current (the leakage current of the transistor is determined by voltage that is biased to it substrate or well. Therefore, the frequency of OSC circuit is also dependent on the leakage current of the transistor. See figure 4); and a control unit (CNT10, CNT20) to maintain a substantially constant ratio between the frequency related to the target frequency and the frequency related to the leakage current (*the ratios between the respective frequencies of the OSC10 and OSC20 and the frequency of CLK10 are constant. Therefore, the ratio between OSC10 and OSC20 is constant*).

As to claim 2, figure 12 shows that the substrate comprises a semiconductor.

As to claim 6, figure 12 shows a self-timed circuit (LOG10) formed on the substrate, the self-timed circuit to operate at a frequency proportional to the target frequency.

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As to claim 7, figures and 12 show that the control unit to provide a control signal to the substrate.

As to claim 8, figures 4 and 12 show that the substrate includes a plurality of coupled wells containing transistors (NMOS) of a matching type from the self-timed circuit, the target timing circuit, and the leakage timing circuit.

As to claim 9, figures 4 and 12 show that the transistors are all of the matching type.

As to claim 10, figures 4 and 12 show a well control unit (the BGEN circuit in CNT10 and CNT20) to provide a bias to the plurality of coupled wells.

As to claim 11, figure 4 shows the well comprises a p-type well.

Claim 12 recites similar limitations of claims 1 and 6. Therefore, it is rejected for the same reasons.

As to claims 13-15, it is seen as an intended use of using circuit LOG10 in a memory, peripheral, or network communication interface.

As to claims 16-18, figure 12 shows that the control unit (CNT10, CNT20) receives signal (S10) having the frequency related to the target circuit frequency and signal (S20) having frequency related to the leakage current.

Claim 26 recites similar limitations of claim 1. Therefore, it is rejected for the same reasons.

As to claim 27, figure 12 shows a processor (OSC30) formed on the substrate and having an operating frequency and a supply voltage (voltage supply to the substrate of transistors in the OSC30), changing the supply voltage to maintain a relationship between the target circuit frequency and the operating frequency.

As to claim 29, figures 4 and 14 shows the step of processing the target circuit frequency and a target ring oscillator frequency to generate a potential control signal to adjust a potential applied to a target ring oscillator, a leakage ring oscillator, and a target circuit that operates at the target circuit frequency.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al. (USP 6166577) in view of Klemmer (USP 6337601).

As to claims 3 and 19, Mizuno et al.'s figure 4 shows that the target timing circuit comprises a ring oscillator. Figure 4 fails to shows that a counter is coupled to the ring oscillator. However, Klemmer's figure 3 shows a timing circuit having counter 82 coupled to the ring oscillator 80 for the purpose of increasing output frequency. Therefore, it would have been obvious to one having ordinary skill in the art to add a counter coupled between the oscillator OSC10 and CNT10 for the purpose of increasing the output frequency of the oscillator OSC10.

As to claim 4, Mizuno et al.'s figures 4 and 12 show that the leakage timing circuit (OSC20) comprises a ring oscillator.

As to claim 5, Mizuno et al.'s figure 12 shows that the frequency related to the leakage current is substantially proportional to the leakage current.

As to claim 20, Mizuno et al.'s figure 4 shows that the leakage ring oscillator comprises delay line.

5. Claims 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al. (USP 6166577).

Figure 12 fails to shows a communication circuit formed on the substrate. However, it is well known in the art that communication circuit operates with clock signal. Mizuno et al.'s figure 12 has the advantage of reduce power consumption. Therefore, it would have been obvious to one having ordinary skill in the art to use Mizuno et al.'s figure 12 in a communication circuit for the purpose of reducing power consumption.

Allowable Subject Matter

6. Claims 21-25 are allowed.

Claims 21-25 are allowable because the prior art fails to teach or suggest the combination of synchronous circuit, target timing circuit, leakage timing circuit, control unit, power source and a potential control unit, wherein the potential control unit receives the signal having the frequency related to the target circuit frequency and the signal having the frequency related to the leakage current and to generate a potential control signal to provide to the power source to adjust the potential.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Quan Tra', is positioned above the printed name and title.

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

June 7, 2005